Jake Hafele

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Objective

Seeking a full-time entry level position for FPGA or Digital ASIC Design starting May 2024.

Education

Iowa State University, College of Engineering

B.S. Electrical Engineering — **December 2023**

GPA: 4.0/4.0

M.S. Computer Engineering — **December 2024**

University of Limerick Study Abroad Program — **Spring 2022**

Employment

Garmin, Design Engineer Intern - Olathe, KS — **May 2023 – August 2023**

- Updated a QSPI entity to communicate with a CPU using a Read/Write interface, from an AXI Lite interface
- Designed a Bus Functional Model using VHDL to read and write QSPI transactions with the FPGA interface
- Defined pinout and timing constraints in Vivado to synthesize an Artix-7 Xilinx FPGA
- Designed a prototype power supply design using Cadence Allegro for a Transponder unit

Iowa State University, Teaching Assistant - Ames IA — **January 2021 – Current**

- Taught courses for classes including Computer Architecture, Digital Logic, and Embedded Systems
- Demonstrated best coding practices in Verilog and C to integrate designs for FPGAs and Microcontrollers
- Analyzed waveforms in ModelSim and real time embedded applications in Code Composer Studio

Collins Aerospace, Systems Engineer Intern - Cedar Rapids, IA — **May 2022 – December 2022**

- Verified software and hardware updates for the CH-47F Chinook platform using system wide tests
- Updated documentation using DOORS that satisfied customer needs and requirements
- Performed system verifications before a software release that ensured system integration met requirements

Skills

Skills	FPGA Synthesis, Waveform Validation, Timing Analysis, Agile Workflow
Tools	Vivado, Quartus Prime, ModelSim, GTKWave, KLayout, Cadence Virtuoso, Git, Subversion
Coding	Verilog, VHDL, C, MATLAB, Python, TCL

Projects

Open-Source Digital ASIC Fabrication

- Designed a silicon proven open-source digital ASIC, with submission and fabrication through eFabless
- Utilized open-source tools such as GTKWave and OpenROAD to verify and layout Verilog designs
- Designed an SPI interface to improve risk mitigation against the provided Wishbone communication bus

Synthesized 5-Stage MIPS Processor

- Utilized ModelSim to build and validate a 5-stage MIPS processor in VHDL
- Performed timing analysis based on instruction count, maximum clock frequency, and cycles per instruction
- Synthesized MIPS processor and I/O using Quartus Prime for an Altera DE2-115 FPGA development board

OLED Display SPI Interface

- Integrated Master write-only SPI Interface in Verilog between FPGA and OLED Display PMOD
- Designed automated testbenches and SPI Bus Functional Model for validation
- Synthesized project in Vivado on Artix-7 FPGA and validated results with real-time ASCII displays

Activities and Leadership

- PrISUm Solar Car Club – Electrical Team Manager
- Critical Tinkers – Leadership Cabinet
- The Engineering Ambassador and Mentor Program

Honors

- Top 2% of Engineers in Class Award — **2020 – 2023**
- College of Engineering Dean's List — **2019 – 2023**